

IN THE TITLE

Kindly delete the originally-presented title and substitute  
therefore the following new title:

--DETECTION APPARATUS FOR DISTINGUISHING BETWEEN ADIP WORD SYNC AND  
ADIP DATA--.

## IN THE SPECIFICATION

Kindly amend pages 1 and 5 of the instant specification as follows:

**Page 1, last paragraph beginning on line 22, please amend as follows:**

The known detection means as shown in Fig. 1 is now further explained in conjunction with the signal diagrams I, II, III, IV, and V as shown in Fig. 2. In the example, the detection of a synchronization bit, which will be further denoted bitsync, in the wobble signal wbl is demonstrated. Diagram I shows the wobble signal wbl. It starts with 3 consecutive sinewave periods between time instants  $t_0$  and  $t_3$ . It is then followed by an inverted sinewave period between time instants  $t_3$  and  $t_4$ . This inverted sinewave period is a bitsync. From time instant  $t_4$  up ~~to~~to  $t_7$  the wobble signal wbl is continued normally, that is to say as if the bitsync did not take place. Also between time instants  $t_7$  and  $t_8$  a bitsync is present in the wobble signal wbl. Diagram II shows the wobble reference signal wblrf which is in fact equal to the wobble signal wbl, such that each bitsync is replaced by a non-inverted sinewave period, so that a monotonic wobble signal is obtained. The generation of the wobble reference signal wblrf may be performed by all known methods, for instance with the aid of a PLL (Phase Locked Loop). Diagram III shows the signal s which is a mathematical

multiplication of the wobble signal  $wbl$  and the wobble reference signal  $wblr_f$ . The signal  $s$  only becomes negative during the bitsyncs in the wobble signal  $wbl$ . Therefore, detection of the bitsyncs is possible in principle by directly coupling the signal  $s$  to a comparator. In practice, however, the signal  $s$  does not have the ideal form as indicated in diagram III. In some cases the signal  $s$  is a (very) noisy signal. As a consequence the comparator may give a false bitsync detection. For this reason the signal  $s$  is first periodically integrated. The integrated signal  $int$  is shown in diagram IV. The length of one time interval  $T_i$  corresponds to one sinewave period. The start and end times of the time intervals  $T_i$  are denoted  $T_B$  and  $T_E$ , respectively. About each start time  $T_B$  the integration means  $INT$  is reset by a start/reset signal  $STRS$  (see Fig.1), and the sample&hold circuit  $SH$  enters in the holding phase. Just (very close) before each ending time  $T_E$  the sample&hold  $SH$  circuit enters in the sampling phase. The resultant further signal  $fs$  is supplied by the sample&hold circuit, and is indicated in diagram V. Now if this integrated signal  $fs$  is coupled to a comparator  $CMP$ , a more reliable bitsync detection is possible.

**Page 5, last paragraph beginning on line 23, please amend as follows:**

Fig. 3a shows a disk-shaped record carrier 1 which comprises a continuous track 9 intended for recording, which track

is arranged in a spiraling pattern of turns 3 around a center 10. The turns may also be arranged concentrically instead of spiraling. The track 9 on the record carrier is indicated by a servo track in which, for example, a pregroove 4 enables a read/write head to follow the track 9 during scanning. A servo track may also be formed, for example, by regularly distributed sub-tracks which, in the servo track system, periodically cause signals to occur. Fig. 3b shows a cross-section taken on a line b-b of the record carrier 1, in which a transparent substrate 5 is covered by a recording layer 6 and a protective layer 7. The pregroove 4 may also be arranged as a land or be a material property that differs from its environment. The recording layer 6 may be deposited in an optical, magneto-optical, or magnetic manner by an apparatus for reading and/or writing information such as the known CD recordable or hard disk for computer use. Figs. 3c and 3d show two examples of a periodic modulation (wobble) of the pregroove. This wobble causes an additional signal to arise in a servo track recorder. A comprehensive description of the CD system comprising disk information can be found in US 4,901,300 and US 5,187,699.